VLSI for SuperComputing from Applications to Algorithms to Masks and Chips

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Abstract:

The objective of this paper is to describe an unconventional way to organize a VLSI design course for future computer engineers. The paper gives a short description of the course content that covers the algorithm-to-mask phase of chip development. It divides VLSI design into three categories: control-flow, data-flow, and wireless-flow. Also, the behavior of students is presented with comments on the influence of this course on their professional life.

1. Introduction

This paper describes a course that teaches VLSI design in an unconventional way. The course tries to stress the following issues:

(a) Experiences of the world's top foundries for VLSI in SuperComputing like Qualcom [1], Intel [2], and Mubadala [3]. Some Toshiba experiences were also taken into consideration [4].

(b) Experiences that will teach Serbian students to become competitive for work openings in the Mubadala R&DFab under development near the Belgrade airport.

(c) Experiences that synergize the phases of a holistic VLSI design, mainly:

- Phase #1: From Applications to Algorithms,
- Phase #2: From Algorithms to Masks, and
- Phase #3: From Masks to Chips.

In this consideration, Phase #1 is just treated by mathematicians, Phase #2 is best treated by computer engineers, and Phase #3 is best treated by physical chemists. Consequently, versions of this course (dialects) are being offered at three different schools of the Belgrade University: The School of Mathematics, The School of Electrical Engineering, and The School of Physical Chemistry.

In each one of its three dialects, this course is stressing the following three issues:

- Deep professional knowledge,
- Detailed multi-dimensional verification, and
- Relevant inter-disciplinary management.

The rest of this paper describes the major elements of the presented course. These elements are the same for each one of its dialects; what differ are teaching examples and homework assignments.

The rest of this paper concentrates on the course dialect of interest to electrical engineering; so, the stress is on the transformation from algorithms to masks.

2. From Algorithms to Implementations

The electrical engineering dialect of the course is divided into three parts:

- Part #1: VLSI for ControlFlow SuperComputing,
- Part #2: VLSI for DataFlow SuperComputing, and
- Part #3: VLSI for WirelessFlow SuperComputing.

Part #1 treats two topics of importance for ManyCore Systems and two topics of importance for MultyCore Systems, as follows:

ManyCore Systems:
- VHDL vs. Verilog (0.5 weeks)
- Design and programming of a 200 MHz microprocessor (2.5 weeks)

MultiCore Systems:
- MicroProcessor and MultiMicroProcessor systems (1 week)
- Testing and verification (2 weeks)

Part #1 is based on references [5] and [6]; also, on standard references related to VHDL and Verilog, (izmena nastavka rečenice) plus verification and testing. The first homework of the course is to use VHDL to describe a processor that is similar to one core of the NVidia Tesla system. The first lab of the course is based on the testing and verification approach of the ELSYS1.

Part #2 treats two topics of importance for FineGrain DataFlow Systems and two topics of importance for SystolicArray DataFlow Systems, as follows:

FineGrain DataFlow Systems:
- Altera vs. Xilinx (0.5 weeks)
- Design and programming of a 200 MHz Maxeler Machine (3.5 weeks)

SystolicArray DataFlow Systems:
- SystolicArray architectures (0.5 week)
- A systolic architecture by DARPA (0.5 weeks)

Part #2 is based on selected parts of references [7] and [8]; also, on standard references related to Altera, Xilinx, DataFlow (Maxeler), and systolic architectures. The second homework of the course is to program a Maxeler application. The second lab of the course is to study the details of the DARPA's implementation of the Gram-Schmidts ortogonalization algorithm.

[1] ELSYS Eastern Europe is a services company specializing in the design of electronic systems as well as in the development of embedded & application software

Part #3 treats two topics of importance for WirelessFlow SuperComputing system design and two topics of importance for the application there of, as follows:

WirelesFlow SuperComputing design: - Hardware (0.25 weeks) - Software (0.25 weeks) WirelessFlow SuperComputing applications: - Ubiquitous computing with Wireless Sensor Networks (0.25 weeks) - DataMining from Wireless Sensor Networks (0.25 weeks)

Part #3 is based on selected references from references [9] and [10]. Homework assignment and lab for this part are optional.

3. Teaching experiences

The bottom line of this course is bringing advanced industrial experience into the classroom. In the first part the experience is oriented to DARPA's first 200 MHz Ga-As microprocessor. In the second part the experience is oriented to the currently most successful DataFlow supercomputer - Maxeler. In the third part the experience is oriented to the EU FP7 project ProSence. Behavior of the students is observed for three different phases of their professional life time:

(a) During the course,

(b) During the first decade after the graduation, and

(c) Around the peak of their professional life time.

During the semester, students complain that the course is difficult. It is rather hard for them to accept the complex content of the course - quite a lot of topics with their in-depth analysis. Also, a lot of time is needed to successfully complete homework and lab examples. For not just a few of them this course was the most demanding one during all their studies.

During the first decade after the graduation they typically say that the know-how from this course helped them impress interviewers at job application processes. Also, the good knowledge of computer design gave them an edge in their overall IT working engagement.

Some of them had chosen VLSI to be their major life orientation. They say that this course created for them a decisive advantage when they were trying to acquire the highest professional positions in the major VLSI industries.

4. References:

[1] Meng, L., Nagalingam, D., Bhatia, C.S., Street, A.G., Phang, J.C.H., "Distinguishing Morphological and Electrical Defects in Polycrystalline Silicon Solar Cells Using Scanning Electron Acoustic Microscopy and Electron Beam Induced Current," *Solar Energy Materials and Solar Cells*, Elsevier B.V., Volume 95, Issue 9, September 2011, Pages 2632–2637.

[2] Rodriguez, D., Espejo, E., Alba, G., Ávila, B., "Development of a Bottom-up Compact Model for Intel®'s High-K 45 nm MOSFET," The *IAENG Transactions on Engineering Technologies* (2013), pp. 123-134.

[3] Al-Hammadi, A. S., Al-Mualla, M. E., Jones, R. C., "Transforming an Economy through Research and Innovation," *University Research for Innovation*, Economica, London, 2013, Glion Colloquium Series N°6, pp. 185 – 197.

[4] Watanabe, S., et al. "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra-high Density DRAM's," *IEEE Journal of Solid-State Circuits*, Sep 1995, Volume 30, Issue 9, pp. 960 – 971.

[5] Milutinovic, V., "Surviving the Design of a 200 MHz RISC Microprocessor: Lessons Learned," *IEEE Computer Society Press*, Los Alamitos, California, USA, 1997.

[6] Milutinovic, V., "Microprocessor and Multimicroprocessor Systems," *Wiley*, 2000.

[7] Sahuquillo, J., Petit, S., Pont, A., Milutinović, V., "Exploring the performance of split data cache schemes on superscalar processors and symmetric multiprocessors," *Journal of Systems Architecture*, Elsevier B.V., Volume 51, Issue 8, August 2005, pp. 451–469.

[8] Milutinovic, V., (editor), "High-Level Language Computer Architecture," *Freeman Computer Science Press*, Rockville, Maryland, 1989. Foreword: M.Flynn (Stanford), Turing laureate, 474 pp.

[9] Gavrilovska, L., Krco, S., Milutinovic, V., Stojmenovic, I., Trobec, R., "Application and Multidisciplinary Aspects of Wireless Sensor Networks," *Concepts, Integration, and Case Studies*, Computer Communications and Networks, 1st Edition., 2011, X, 282 p., Hardcover, ISBN: 978-1-84996-509-5.

[10] Rakocevic, G., Djukic, T., Filipovic, N., Milutinović, V., "Computational Medicine in Data Mining and Modeling," Springer, New York, 2013, ISBN 978-1-4614-8785-2.